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| 09/659,872 | 09/13/2000 | Hartmund Terletzki | 00P7882US | 7001 |

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| EXAMINER |
|---|
| NGUYEN, MINH T |

| ART UNIT | PAPER NUMBER |
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| 2816 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/659,872 | Applicant(s) TERLETZKI ET AL. | |
|---|---|---|---|
| | Examiner Minh Nguyen | Art Unit 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6* is/are allowed.

6)☒ Claim(s) *1-5,7-13,15,18,20-28 and 30* is/are rejected.

7)☒ Claim(s) *14,16,17,19 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Amendment*

1. Applicants' amendment filed on 4/12/02 has been received and entered in the case. The amendment and argument presented therein overcome the informality objections and indefiniteness rejections, and therefore, are withdrawn. New ground of rejections necessitated by the amendment is set forth below. This action is FINAL.

### *Claim Objections*

2. Claims 14 and 23 are objected to because of the following informalities:

In claim 14, line 5, "a fifth p-channel" should be changed to -- a sixth p-channel --.

In claim 23, "current path current path" recited on lines 2 and 5 should be changed to -- current path--,

"third reference voltage" recited on line 3 should be changed to --first reference voltage--,

"first reference voltage" recited on line 6 should be changed to --third reference voltage--.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,216,390 to Stewart.

As per claim 1, Stewart discloses a level shifting circuitry (Fig. 1) comprising:

a level shifting section (circuits 10, 12 and 14) responsive to an input logic signal (the input signal at node 20), the limitation that the input logic signal having a first voltage level representative of a first logic state "1" and a second voltage level representative of a second logic state "0" is only given patentable weight to the extent that if the Stewart level shifting section is capable of receiving such a signal, the limitation is met, and since it is clear that the Stewart level shifting section is capable of receiving the recited input logic signal, the recited limitation is met (MPEP 2114, i.e., in a circuit claim, the claimed circuit must be distinguished from the prior art in term of structure rather than a manner to operate the circuit), and providing an output logic signal (the signal at node 30) at an output terminal 30, the recited limitation that the output logic signal having a third logic voltage level representative of the first logic state of the input logic signal and a fourth voltage level representative of the second logic state of the input signal is met since it is merely the result when the Stewart level shifting section is operated (MPEP 2112.01, i.e., when the structure of the claimed circuit and the reference circuit are substantially identical, claimed properties and/or functions are presumed to be inherent);

an enable/disable section 16 coupled to the level shifting section wherein the level shifting section responsive to an enable/disable signal Vc for placing the output terminal 30 to a high output impedance condition (when transistor P3 is OFF) independent of the logic state of the input signal during a disable mode.

As per claim 7, the recited additional transistor reads on transistor P26 which is connected as recited.

As per claim 8, since transistor N3 is N-type and transistor P26 is P-type, the recited limitation is met.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 9-13, 15, 18, 20-28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,216,390 to Stewart.

As per claim 2, Stewart discloses a level shifting circuitry (Fig. 1) comprises elements and connections as discussed in claim 1 above wherein the level shifting circuitry includes:

an input transistor N3 having a first electrode 22 coupled to the input logic signal 20, and a second electrode (at node 28);

a first switching transistor P3;

an output pair complementary transistors P1b and N1b wherein P1b having a first electrode 34 coupled to the source of the third voltage level V3 through the first switching transistor P3, a control electrode coupled to the second electrode of the input transistor N3 at node 28, a junction 30 and wherein the control electrode of N1b is connected to the second

electrode of the input transistor N3 and the second electrode of the second one of the output transistors N1b is directly coupled to ground.

Stewart does not explicitly teaches the level shifting section in Fig. 1 further includes a second switching transistor and the second one of the pair transistor having a second electrode coupled to a source of a second voltage level through the second switching transistor as called for in the claim.

Stewart discloses another level shifting circuit (Fig. 3) having a second switching transistor N5A, and he further teaches that when the input logic signal swings in a negative region (column 4, line 31), i.e., the second voltage level is negative, a second switching transistor N5A should be added (column 4, lines 30-60).

It would have been obvious to one skilled in the art at the time of the invention was made to include a second switching transistor taught in Fig. 3 of the Stewart reference to the Stewart's level shifting section shown in Fig. 1.

The motivation/suggestion for doing so would have been to allow the Stewart's level shifting circuit shown in Fig. 1 to function when the levels of the input logic signal is either positive or negative.

Therefore, it would have been obvious to add the second switching transistor to Fig. 1 of the Stewart reference to obtain the invention as specified in claim 2.

As to the limitation that the first and second switching transistors are fed by the enable/disable signal. This limitation would have been obvious also since the first and second switching transistors must be both ON or OFF during any period of time, therefore, by using

only one signal, this requirement can be obtained. A further motivation would have been by using a single signal, the control section would be simpler.

As per claim 3, the recited limitation that the enable/disable section includes an inverter is met because as shown in Fig. 1 and 3, the first switching transistor P3 is P type and the second switching transistor N5A is N type, therefore, when using only the enable/disable signal to turn ON or OFF both of these transistor, an inverter must be included.

As per claim 4, since it is clear that the inverter discussed in claim 3 above must be powered by a voltage source, and the inverter can be operated when the voltage source is held at the first voltage level, the recited limitation is met.

As per claim 5, the combination discussed in claim 4 above discloses that the control electrode of the input transistor N3 is coupled to a source having a voltage level V2 as shown in Fig. 1 of the Stewart reference but does not explicitly disclose that this source is the same as the source providing the power for the inverter. However, it is old and well-known that it is desirable to use a same source to supply power for a circuit because it is more convenience and it requires less space. It would have been obvious to one skilled in the art at the time of the invention was made to use the same source to provide the power for the control electrode of the input transistor and the inverter for the obvious advantage discussed herein above.

As per claim 9, this claim is rejected for the same reasons and motivations noted in claim 2 above wherein the recited input node reads on node 20, the recited input signal reads on the signal provided by the source 9; the recited first n-channel transistor reads on transistor N1b, the recited second n-channel transistor reads on transistor N5A coupled to the second voltage level reference node V2A and a gate coupled to the first enable signal node (the node which connects

to the signal VC1); the recited first p-channel transistor reads on transistor P1b; and the recited second p-channel transistor reads on transistor P3 which is coupled to a third reference node V3 and a gate coupled the a second enable signal node (the node which provides the signal VC); the limitation that the third voltage level being different than the first voltage level is only given patentable weight to the extent that if the Stewart's second p-channel transistor is capable of receiving such a voltage level, and since it is clear that P3 can receive a third voltage level which is being different than the first voltage level, the recited limitation is met.

As per claim 10, the recited third n-channel transistor reads on N3 wherein the first voltage reference node reads on node 26.

As per claim 11, the recited third p-channel transistor reads on P26.

As per claim 12, this claim is rejected for the same reason noted in claim 3.

As per claim 13, the circuit discussed in claim 12 above comprises an inverter for providing the enable/disable signal to the second enable node but does not disclose that the inverter comprises a p-channel and an n-channel transistors and the p-channel transistor is powered by connecting to the first voltage level reference node as called for in the claim.

The examiner take Official Notice that implementing an inverter using a p-channel and an n-channel transistors connected as recited in the claim is old and well-known in the art.

It would have been obvious to one skilled in the art at the time of the invention was made to implement the inverter recited in claim 12 using a p-channel and an n-channel transistors connected as recited for the advantage that using the old and well-known way, the skilled worker does not have to waste time to design the inverter.

As to the limitation that the p-channel is powered by connecting to the first voltage level reference node, this limitation would have been obvious also since by connecting to an existing node to receive the power source, only a single power supply is needed.

As per claim 15, since the second enable signal node receives the signal through the inverter, the recited limitation is met.

As per claim 18, the configuration discussed in claim 9 above clearly requires the third voltage level greater than the first voltage level.

As per claim 20, this claim is rejected for the same reasons and motivation noted in claim 9 above wherein the recited first reference voltage node reads on the node which is connected to the drain of transistor N5A which carries the voltage level V2A, and since the drain of N5A can receives the voltage level V2A which is the first voltage level, the recited limitation is met; the recited third reference voltage node which carries the third voltage level reads on node 36; the recited first potion reads on transistor N5A and the recited second portion reads on transistor P3, and these portions are connected as recited.

As per claim 21, the recited limitations are always met since they are merely the definitions of the first and third voltage levels, i.e., defining the first and third voltage levels as first and second logic states, respectively, and the limitations are met.

As per claim 22, the recited first and second transistors read on N1b and P1b, respectively.

As per claim 23, the recited third and fourth transistors read on transistors N5A and P3, respectively, and there transistors are connected as recited.

As per claim 24, the recited limitation is merely the result when the circuit is operated, and since the prior art circuit discussed in claim 23 has all the recited structure, the recited limitation result is clearly met.

As per claim 25, the recited first and second switches read on transistors N5A and P3, respectively.

As per claims 26-28, these claims are rejected for the same reasons noted in claims 3, 3, 13, respectively.

As per claim 30, it is clear that transistors N5A and P3 are MOS transistors.

***Response to Arguments***

5. Applicant's arguments filed 4/12/02 have been fully considered but they are not persuasive.

Regarding the argument that Stewart does not teach or suggest the enable/disable section places the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode. The examiner notes that as discussed in the preceding rejection, the enable/disable section reads on transistor P3 which is when an input voltage to the gate of P3 is LOW, the output terminal 30 is at low output impedance and when the input voltage to the gate of P3 is HI, the output terminal 30 is at high output impedance independent of the logic state of the input logic signal, and the recited limitation is met.

Regarding the argument that the reference does not teach any condition where the terminal 30 is placed at a relatively high output impedance condition. The examiner notes that

the teaching is shown in Fig. 1. The Applicants are reminded that the drawings must be considered as part of the disclosure.

Regarding the argument that the control circuit 16 is merely for selectively changing the operating potential applied to latch 12. This argument is not found persuasive because the Applicants fail to show why the claimed enable/disable circuit and the prior art enable/ disable circuit both have the same structure, but the prior art circuit cannot functioned as the claimed circuit. In order for the argument to be persuasive, the Applicants need to show either the function of the enable/disable circuit recited in the claim resulting in different structure from the reference circuit or the prior art circuit cannot perform the function recited in the claim (MPEP 2112.01).

***Allowable Subject Matter***

6. Claim 6 is allowed.

Claim 6 is allowed because the prior art of record fails to disclose or suggest a level shifting circuit which includes a level shifting section and an enable/disable section wherein the enable/disable section includes an inverter which comprises a level shifter circuit for shifting the enable/disable signal from a first voltage level to a third voltage level as recited in the claim.

7. Claims 14, 16-17, 19 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 14 is allowable for the same reason noted in claim 6, i.e., the fifth and sixth transistors is a level shifter circuit.

Claims 16-17, 19 and 29 are allowable for the same reason noted in claim 6.

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MN
June 11, 2002

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800